

## ADN2848 AC-Coupled Optical Evaluation Kit

By Mark Murphy, Ferenc Barany, and Michael O'Flanagan

### INTRODUCTION

This application note describes the 32-lead ADN2848 laser diode driver Rev. A1 evaluation kit. The evaluation kit is a demonstration board that provides ac-coupled optical evaluation of the ADN2848. This document describes how to configure the board in order to operate this part optically. The document contains the following information:

- Board description
- Quick start for optical operation
- Description of board settings
- Component list
- Schematic of board
- Board layout information
- Silkscreen image of board

### BOARD DESCRIPTION

The ADN2848 is a 3V dual-loop 50 Mbps to 1.25 Gbps laser diode driver. To use the board in an optical configuration, a suitable laser diode driver must be soldered onto the board. The monitor photodiode, MPD, current is fed into the ADN2848 to control the average power and extinction ratio. The ADN2848 uses automatic power control, APC, to maintain a constant average power over time and temperature. The ADN2848 also uses closed-loop extinction ratio control to allow optimum setting of extinction ratio for every device. This board is configured for lasers in mini-DIL packages only. LEDs for Power Supply, DEGRADE, and FAIL are made available for monitoring purposes. **Power to the ADN2848 evaluation circuitry is only –3.3 V.**

### QUICK START FOR OPTICAL OPERATION

To ensure proper operation in the optical configuration, verify the following:

1. Jumpers K3 and K4 are connected to A; Jumper K2 is connected to B.
2. If the input data is clocked, it is necessary to enable the clock select pin (CLKSEL). CLKSEL is enabled by connecting K4 to B. If the clock inputs are not used, or if the input data is not latched, connect K4 to A.
3. The power supply is diode protected to ensure the device is not damaged if a positive power supply is accidentally connected. The user may connect Jumper K1 (short circuit)

and power up the board by applying –3.3 V to the POWER input SMA, J3. If Jumper K1 is not connected, the user should make the power supply sufficiently negative to ensure that the supply is –3.3 V. The actual DUT supply can be measured at the anode of D1.

4. Apply a differential signal, typically 500 mV, to J6 and J7 (DATAN and DATAP). Single-ended operation may result in a degraded eye.
5. If the clock select pin is enabled by K4, apply a differential clock signal, typically 500 mV, to J4 and J5 (CLKN and CLKP). If the clock pin is not enabled, a clock signal should not be connected.
6. The optical eye and switching characteristics of the ADN2848 may be observed using a digital communications analyzer that has an optical input channel with the required bandwidth.
7. The bias and modulation currents can also be monitored by observing IBMON and IMMON, respectively. IBMON and IMMON are both a 1:100 ratio of  $I_{BIAS}$  and  $I_{MOD}$ . Both are terminated with resistors and so can be viewed at Test Points T3 and T4 using a voltmeter or oscilloscope.
8. To establish the desired average power and extinction ratio, the user should follow this procedure:
  - a. With the power supply turned off, adjust Potentiometers R20 (ERSET) and R21 (PSET) to approximately 20 k $\Omega$ .
  - b. With the evaluation board powered on and the data signal switching, the user can reduce the value of Potentiometer R21 to establish the desired average optical power.
  - c. Potentiometer R20 can then be reduced in value to increase the modulation current, and thus increase the extinction ratio. The bias and modulation currents can be monitored using IBMON and IMMON.

When adjusting the extinction ratio, the user should allow adequate time for the eye to settle. The allowable resistance range at the power set input (PSET), the Extinction Ratio Set Input (ERSET), and the Alarm Set (ASET) is between 1 k $\Omega$  and 25 k $\Omega$ . Resistors R31 through R33 ensure that the resistance at these nodes never falls below the minimum allowable value. If the node resistances increase above 25 k $\Omega$ , the ADN2848 may not operate within its specifications.

Table I. Description of Board Settings

Component	Name	Function
J3	POWER	-3.3V Power Input to Board
J4	CLKN	CLKN Input
J5	CLKP	CLKP Input
J6	DATAP	DATAP Input
J7	DATAN	DATAN Input
T1	IMPDMON	IMPD Current Mirror Monitor
T3	IBMON	Bias Current Mirror Monitor
T4	IMMON	Modulation Current Mirror Monitor
R19	ASET Potentiometer	Adjusts Bias Threshold Current for Degrade and Fail Alarms
R20	ERSET Potentiometer	Adjusts the Extinction Ratio
R21	PSET Potentiometer	Adjusts the MPD Current and Thus the Average Power
K1	K1	Jumper to Bypass Supply Protection Diode
K2	K2	Jumper for LBWSET
K3	K3	Jumper to Exercise ALS
K4	K4	Jumper for CLKSEL

Table II. Component List

Component	Quantity	Description
R19, R20, R21	3	50 k $\Omega$ Trim Potentiometers
D1	1	Supply Protection Diode (1N4001)
D2, D3, D4	3	SMD LEDs
C3–C11, C16–C18	12	10 nF Capacitors
C2	1	220 $\mu$ F Capacitor
C13, C14	2	1 $\mu$ F Capacitors (Loop Bandwidth Setting)
C15	1	1 pF Capacitor
C19 <sup>1</sup>	1	Not Populated
C12, C20 <sup>2</sup>	2	220 nF
Q3, Q4	2	Transistors (SOT23)
C1	1	22 $\mu$ F
R15, R18	2	10 k $\Omega$ Resistors
R3	1	10 $\Omega$ Resistor
R5	1	100 $\Omega$ Resistor
R2	1	24 $\Omega$ Resistor
R1, R16, R17	3	330 $\Omega$ Resistors
R4 <sup>1</sup> , R7 <sup>1</sup> , R8 <sup>1</sup>	3	Not Populated
R31–R33	3	820 $\Omega$ Resistors
R11, R13, R14	3	1.5 k $\Omega$ Resistors
R25, R26 <sup>1</sup> , R28	3	0 $\Omega$ Resistors
K1–K4	4	Pin Header Jumper Sockets
J3–J7	5	SMA Connectors
U1	1	ADN2848
U2 <sup>1</sup>	1	Laser Diode—Not supplied by Analog Devices
L1, L2	2	10 $\mu$ H Inductors
L4, L6	2	100 $\mu$ H Inductors
L3, L5	2	1 $\mu$ H Inductors

## NOTES

<sup>1</sup>Components that are not populated.

<sup>2</sup>The values of C12 and C20, the ac coupling capacitors, and Inductors L3 through L6 to IMODP and IMODN may be experimented with by the user. Changing the values of these capacitors may improve or degrade the pattern dependency of the circuit and may have implications on the jitter performance.

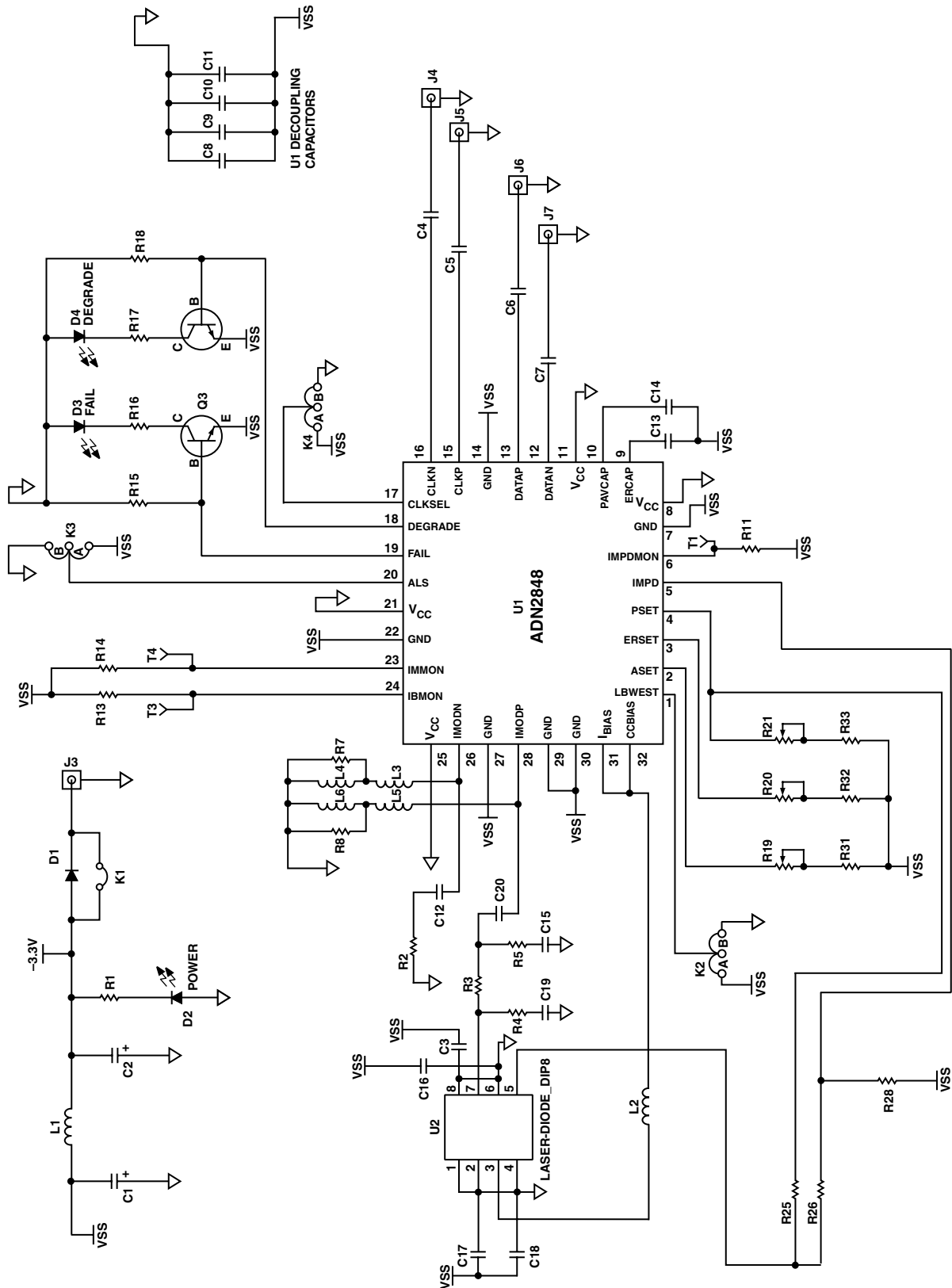


Figure 1. Schematic of Board

## BOARD LAYOUT

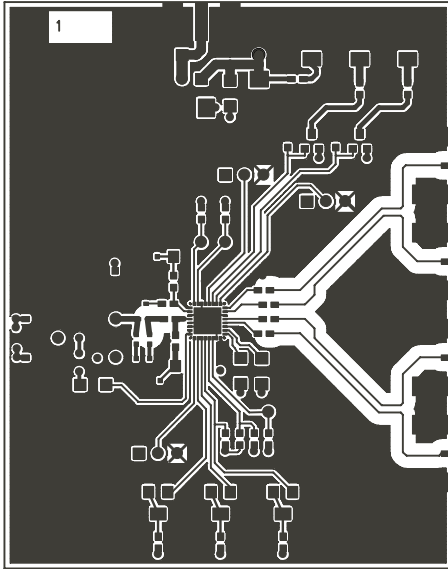


Figure 2. PC Component Side

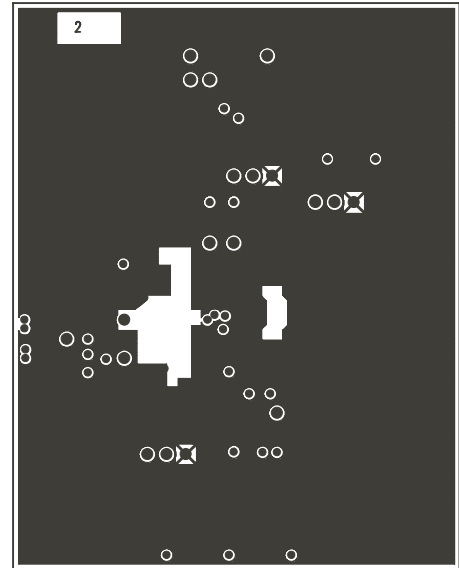


Figure 4. PC Ground Plane

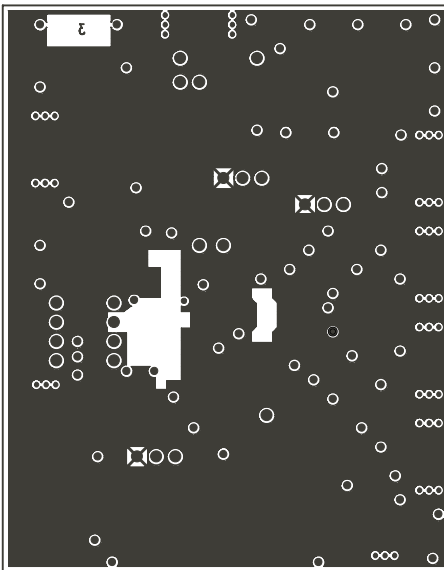


Figure 3. -5V/-3.3V Power Plane

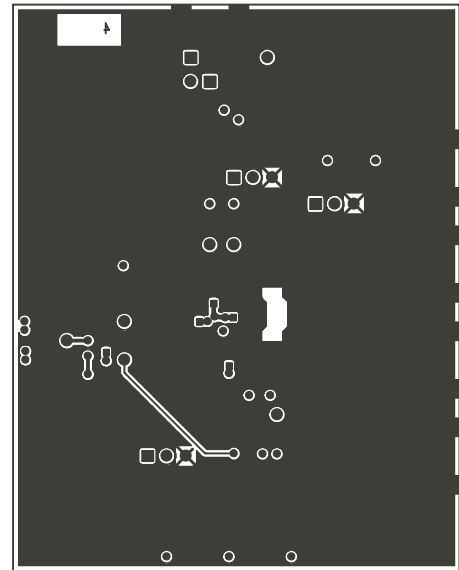


Figure 5. Solder Side

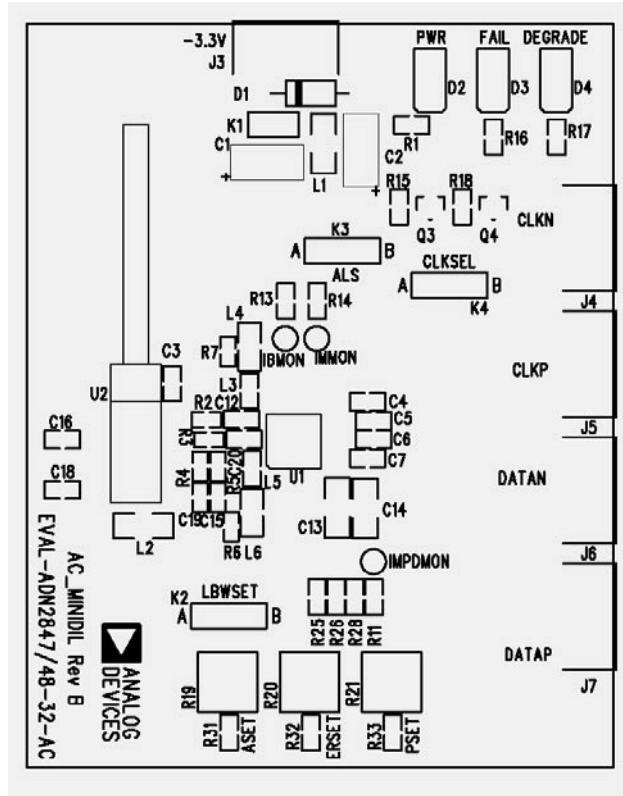


Figure 6. Silkscreen Image



